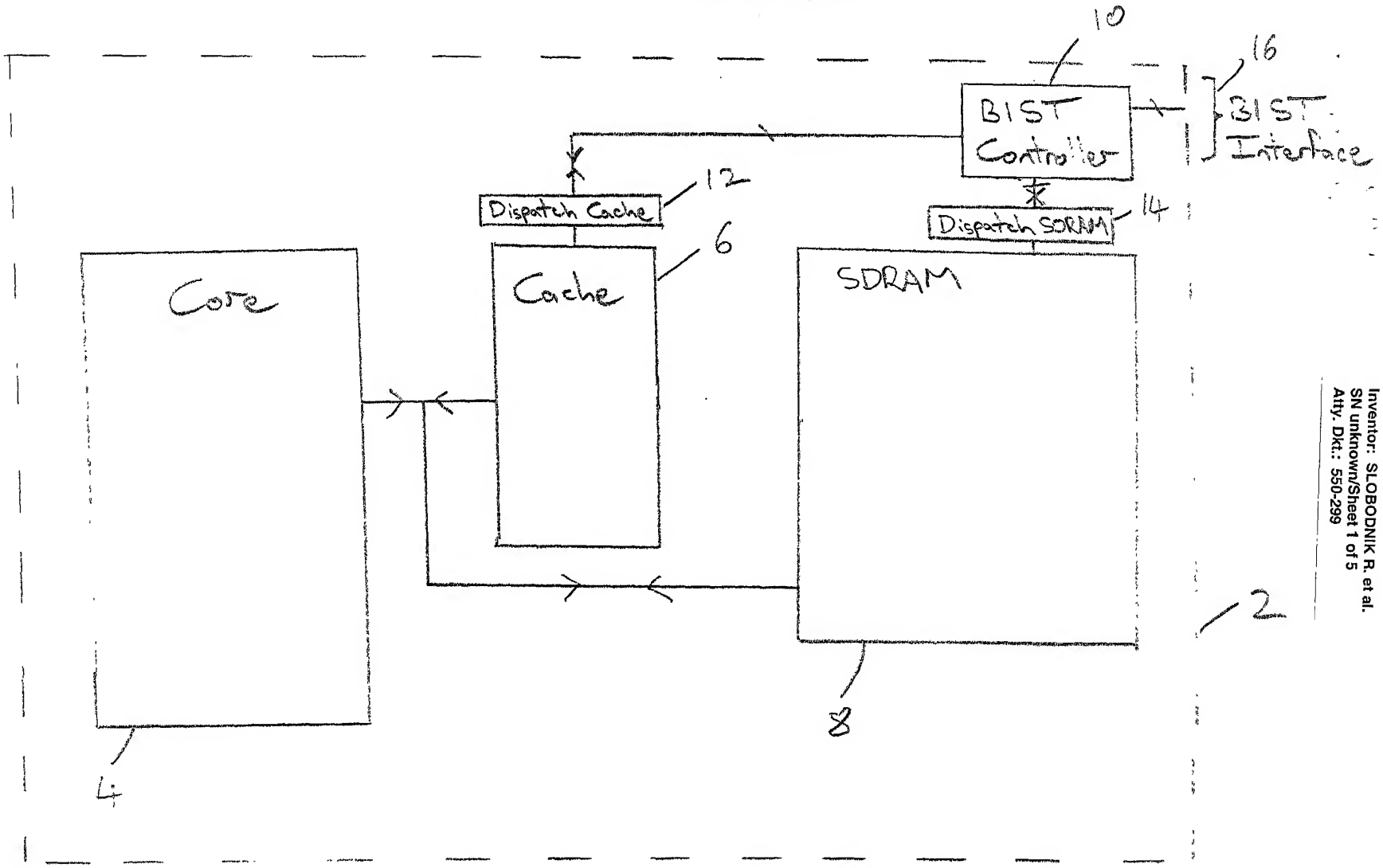


Fig. 1

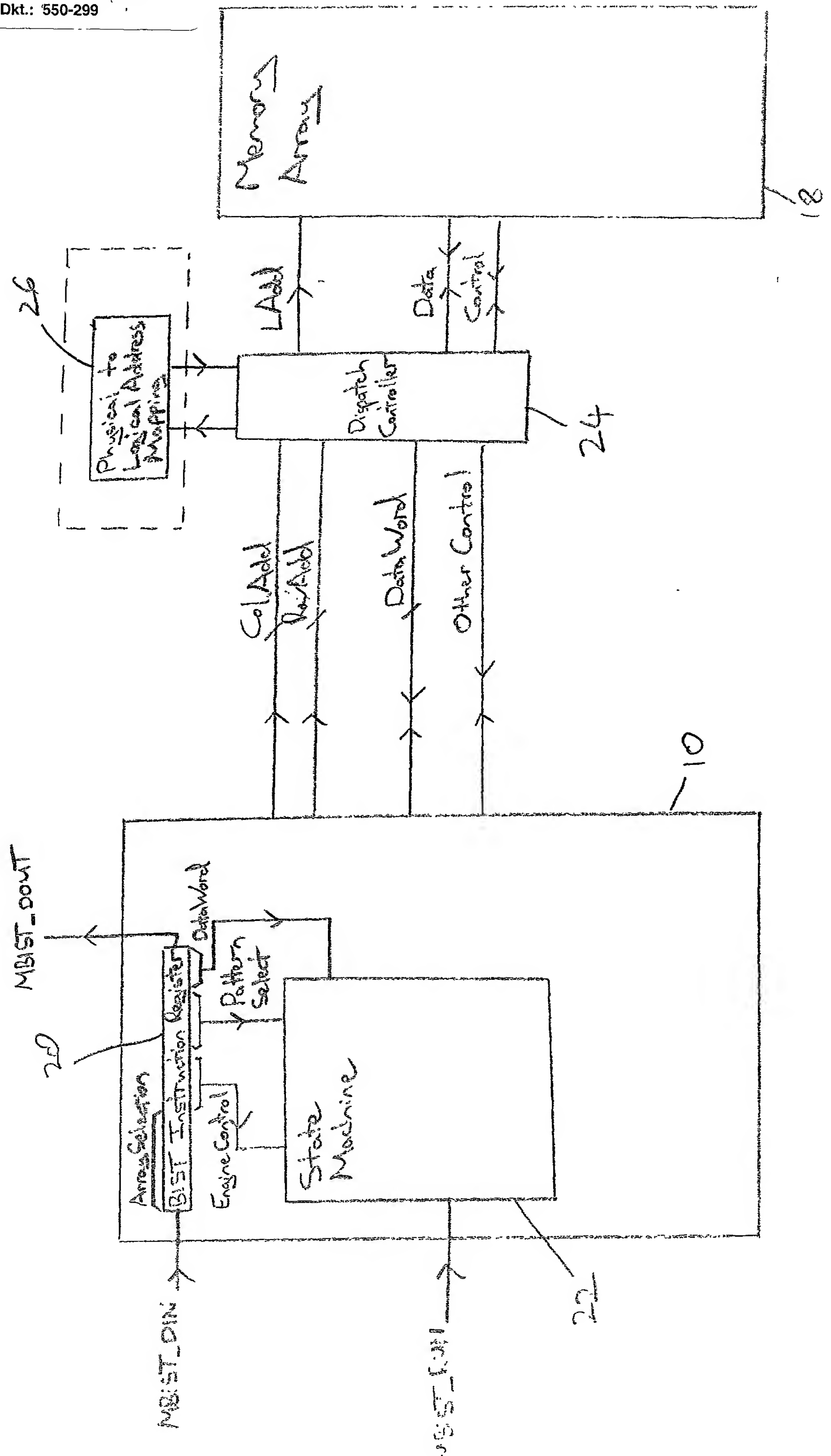

Memory Array
18
LAdd
Data
Control
26
Physical to Logical Address Mapping
Dispatch Controller
24
ColAdd
RowAdd
Data Word
Other Control
10
MBIST_DOUT
Data Word
Pattern Select
20
BIST Instruction Register
Array Selection
Engine Control
State Machine
22
MBIST_DIN

Fig. 2

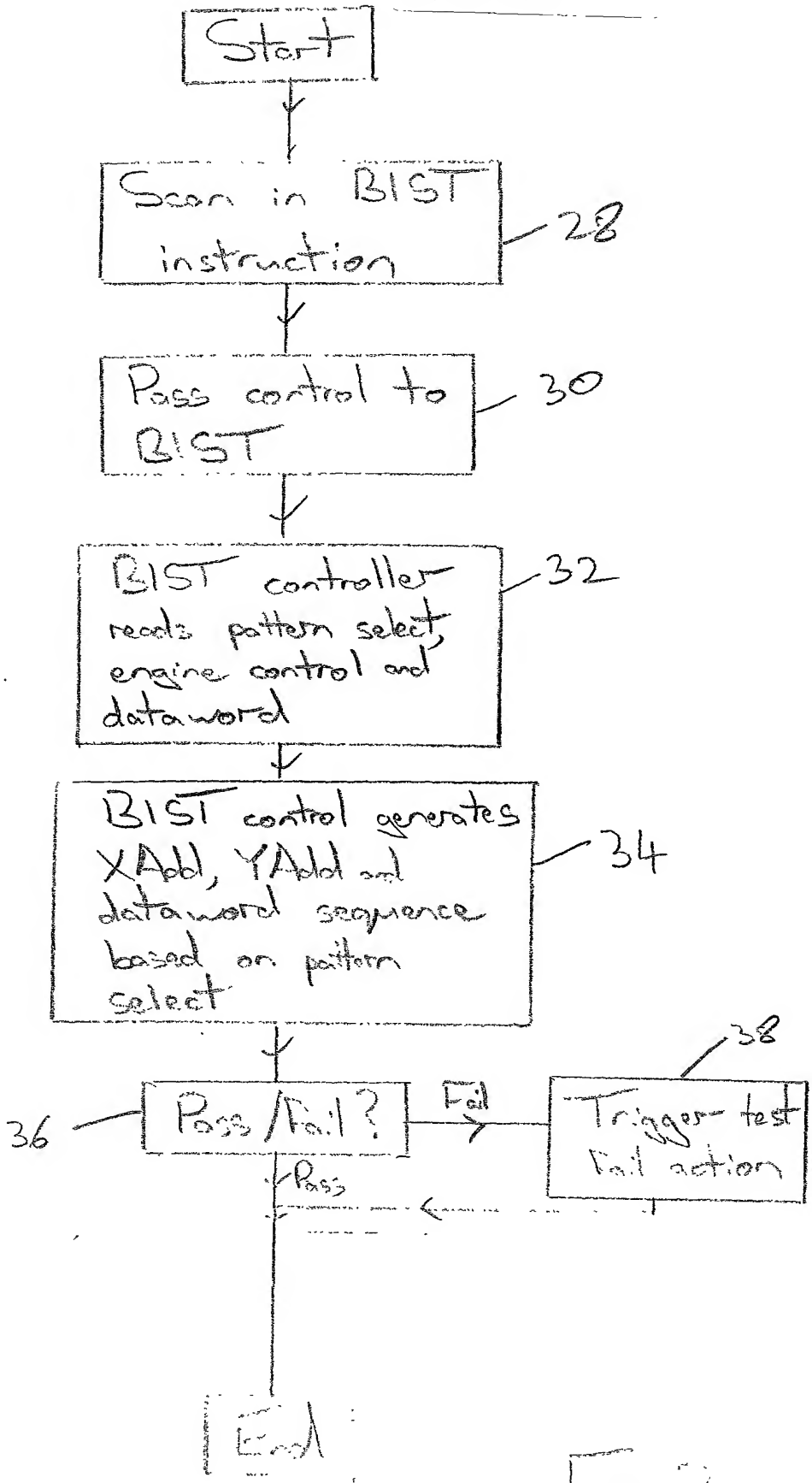


Fig. 3

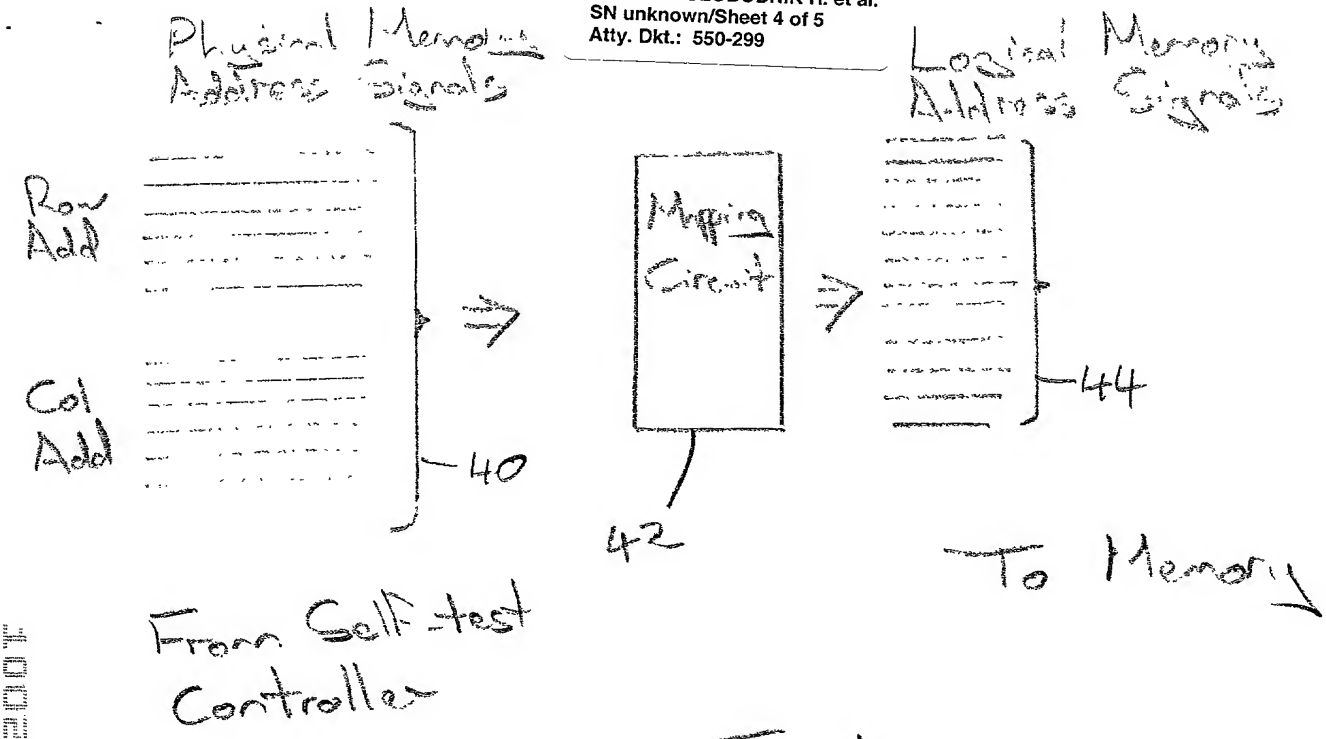
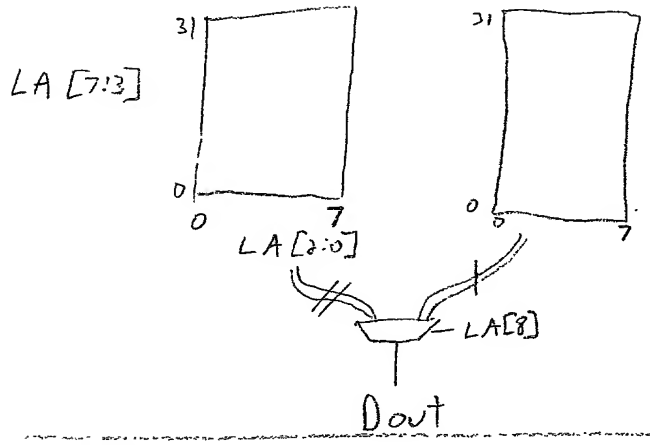

Physical Memory Address Signals
Logical Memory Address Signals
Row Add
Col Add
40
Mapping Circuit
42
44
From Self-test Controller
To Memory

Fig. 4

LA [8:0] when implemented has 32 rows, 8 cols, 1 block select



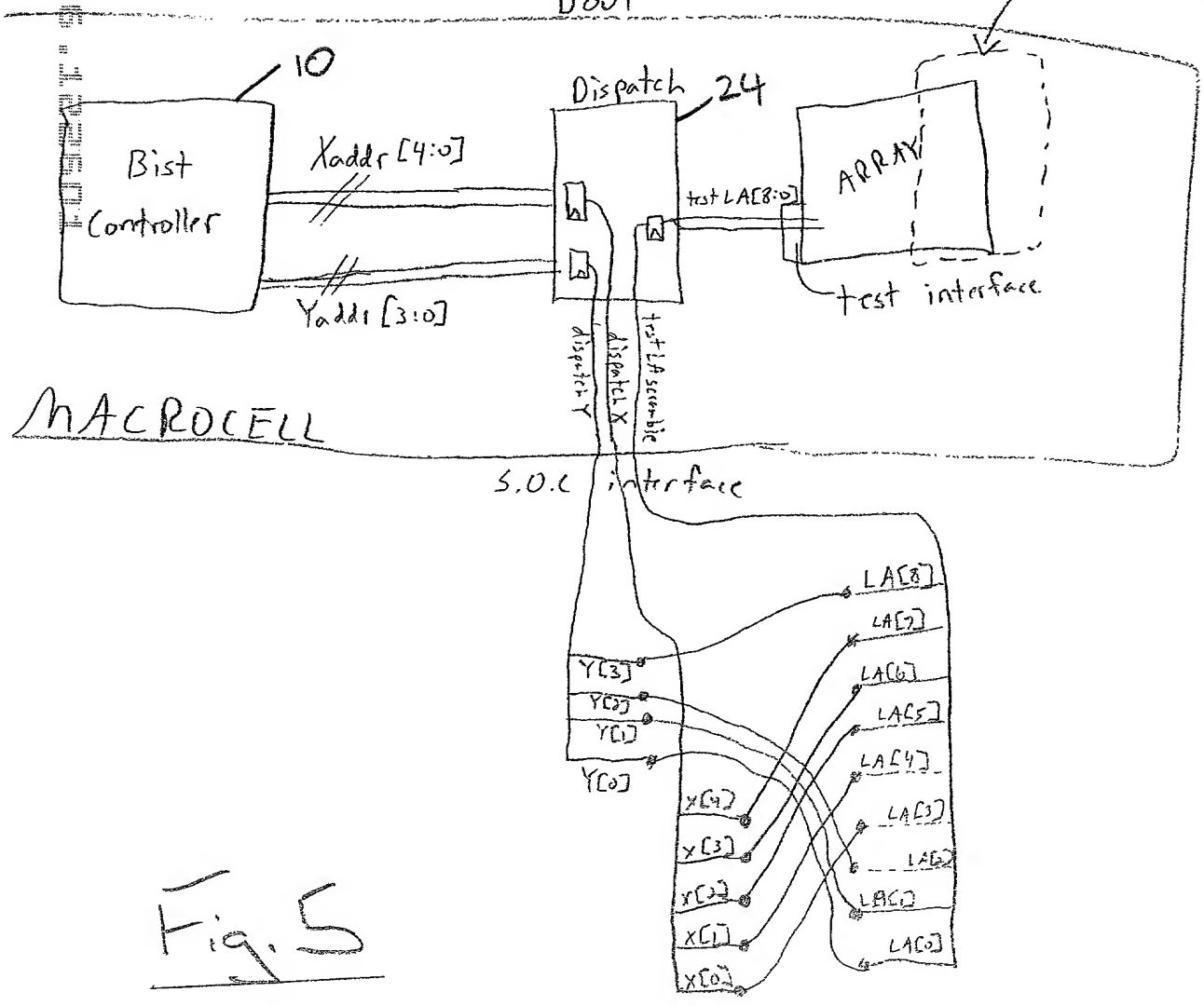


Fig. 5